CUSTOMIZED SHIELD PLATE FOR A FIELD EFFECT TRANSISTOR

BACKGROUND

[0001] 1. Field of Disclosure

[0002] The disclosed subject matter is in the field of semiconductor devices and, more particularly, field effect transistors.

[0003] 2. Related Art

[0004] Shield plates have been used in conjunction with field effect transistors to control or modify electrical fields that the transistors generate during operation. The values of parasitic elements associated with conventional shield plates were largely determined by fabrication process parameters. While designers could specify how far a shield plate extended beyond the gate electrode sidewall parallel to the surface region of the underlying substrate, this parameter was subject to a minimum below which the structure would lose its effectiveness as a shield plate. Thus, designers were constrained in their ability to reduce the parasitic capacitance associated with a shield plate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

[0006] FIG. **1** is a layout of a transistor employing a conventional field plate according to the prior art;

[0007] FIG. **2** is a cross section illustrating selected elements of a field effect transistor including a customized shield plate;

[0008] FIG. **3** depicts additional detail of a portion of the transistor of FIG. **2**;

[0009] FIG. **4** is a layout view of selected elements of a field effect transistor having a customized shield plate;

[0010] FIG. **5** is a cross section of an implementation employing multiple field plates; and

[0011] FIG. **6** depicts aspects of the cross section of FIG. **4**.

DETAILED DESCRIPTION

[0012] Referring to FIG. **1**, a layout view of selected elements of a transistor **10** is depicted. As depicted in FIG. **1**, transistor **10** includes a gate electrode **11** positioned between a source region **20** and a drift region **14**. Drift region **14** extends from gate electrode **11** to a drain region **22**. Gate electrode **11** includes a first sidewall **12** proximal to source region **20** and a second sidewall **13** proximal to drain region **22**. Transistor **10** includes a Faraday shield plate, identified as shield plate **15**, used to improve control of electrical fields and achieve higher breakdown voltage. Shield plate **15** overlies second sidewall **13** and extends from a first boundary **16** overlying gate electrode **11** to a second boundary **17** overlying drift region **14**. In the configuration depicted in FIG. **1**, second boundary **17** of shield plate **15** is substantially parallel to second sidewall **13** of gate electrode **11**, with a displacement D**0** between gate electrode second sidewall **13** and shield plate second boundary **17**.

[0013] The configuration of shield plate **15** as depicted in FIG. **1** results in a capacitive structure that affects the operation of transistor **10**. Moreover, the value or magnitude of the capacitor is, at least to some extent, predetermined by the fabrication process, which dictates, for example, the vertical displacement between shield plate **15** and the underlying drain region **14**. Disclosed below is a shield plate configuration that permits a degree of control over the electrical characteristics of the shield plate.

[0014] In one embodiment, disclosed subject matter describes a semiconductor device that includes a plurality of transistors fabricated or otherwise included in a packaged semiconductor die. The transistors include at least one transistor referred to herein as a customized shield plate field effect transistor (FET). The customized shield plate FET includes a semiconductor layer, a gate dielectric, a gate electrode, an interlevel dielectric (ILD) referred as a shield ILD, and at least one shield plate referred to herein as a customized shield plate. The semiconductor layer may be an epitaxial layer formed on a semiconductor substrate. The semiconductor layer includes a surface layer, extending from an upper surface of the semiconductor layer to a predetermined depth, that represents a region in which source and drain regions of the FET are formed.

[0015] The gate dielectric may be a thermally formed silicon oxide, another material having a suitable high dielectric constant, or a combination thereof. The gate electrode includes a first sidewall and a second sidewall that define lateral boundaries of a channel region of the surface layer underlying the gate electrode. The channel region is laterally displaced within the surface layer between a source region and a drain region of the surface layer. The gate electrode may be a doped polysilicon, another sufficiently conductive material including a silicide material, or a combination thereof.

[0016] The shield ILD includes a shield portion overlying at least a portion of an upper surface of the gate electrode, the sidewall, referred to herein as the d-sidewall, of the gate electrode proximal to the drain region, and a portion of the drain region. The customized shield plate includes a conductive film, such as a metal, silicide, or other suitable material, overlying the shield portion of the shield ILD. The shield plate defines or includes an edge, referred to herein as a customized shield plate edge, that overlies the drain region of the surface layer in the semiconductor substrate.

[0017] The shield plate edge may be configured so that a distance between the shield plate edge and the d-sidewall of the gate electrode varies along a length of the d-sidewall. The variation in distance may be achieved by fabricating the shield plate edge as a series of line segments forming triangular elements or elements of other shapes. In other configurations, the shield plate edge may include semicircular or other curved-edge elements. The configuration of the shield plate edge may be designed to achieve a desired value of a parasitic capacitance or other parasitic element or characteristic of the FET. The shield plate edge might, for example, be configured to reduce the total area of the shield plate and thereby reduce the parasitic capacitance of the shield plate. Any reduction in capacitance cannot, however, be accompanied by a reduction in the device's performance or reliability.

[0018] The customized shield plate FET may be implemented as a lateral diffused metal oxide semiconductor (LDMOS) transistor. The customized shield plate FET may include two or more shield plate structures, separated by intervening shield plate ILDs. When multiple shield plates are employed, one or more of the shield plates may include a customized shield plate edge. The spacings between shield